LV1020

0.50 inch Quad VGA µOLED Display Module (61-pin FPC, 59.94 fps)

Description

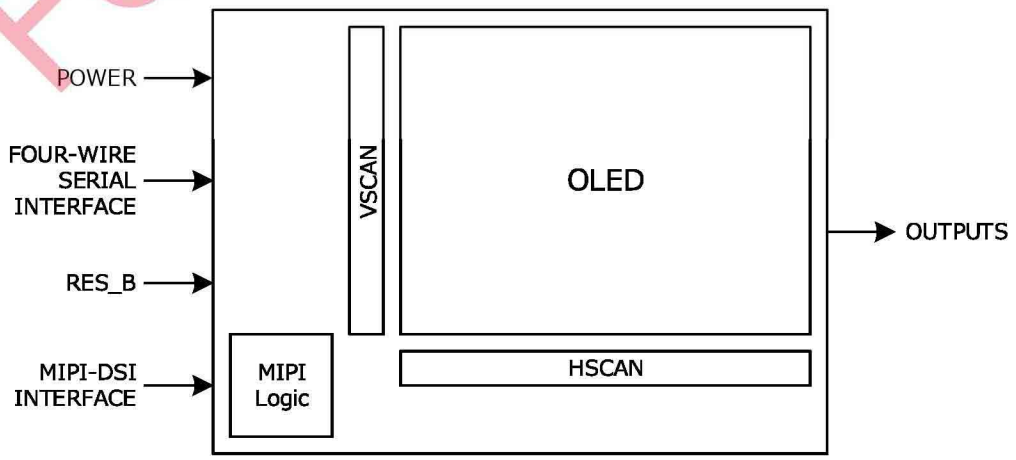
This µOLED Display Module has a 0.50 inch display size, Quad VGA (1280 x 960) resolution, and a pixel pitch of 7.8 µm.

This Data Sheet is a PRELIMINARY version, so the "TBD" notation indicates items that contain undetermined values.

Features and Functions

- OLED panel with active matrix type on-chip color filter
- Display size: 0.50 inch
- Number of pixels: 1280 (H) x 960 (V) = 1,228,800 pixels
- Number of display dots: 1280 (RGB) x 960 = 3,686,400 dots (excluding the orbit area)
- Pixel size: 7.8 µm x 7.8 µm (dot size depends on the dot array)
- Color reproduction gamut (TBD): sRGB area ratio 94%
  (Typ., 500 cd/m^2, area ration on a u'v' chromaticity diagram)
- Whit point: D65 reference
- Display gradations (TBD): 1024 gradations (8bit + FRC) for each color
- Brightness (TBD): 1,000 cd/m^2 (Maximum Luminance), 180 cd/m^2 (Standard Luminance)
- Contrast Ratio (TBD): 100,000 : 1 (Maximum Luminance)
- γ curve: γ = 2.2 ± 0.2 (applied to the range with 32 of or more gradations at the standard brightness setting)
- Frame rate (TBD): 59.94 fps progressive (RGB 24bit), 119.88 fps pseudo interlace (RGB 24bit)
- Power consumption: 265 mW (Typ., 180 cd/m^2, 59.94 fps progressive)
- Video interface: conforms to MIPI-DSI v1.2, CLK 1 Lane + Data 3 Lane, 648 Mbps
- Control interface: 4-wire serial communication
- Orbit processing function: 20 pixels each horizontal and vertical
- Digital γ correction using the FRC (Frame Rate Control) function
- Power supply voltages: 10 V, 1.8 V
- 61 pin FPC (Flexible Printed Circuits)
- Module size: 17.88 mm x 15.28 mm x 6.24 mm (not including flexible cable part)

Functional Block Diagram



1. Display Structure

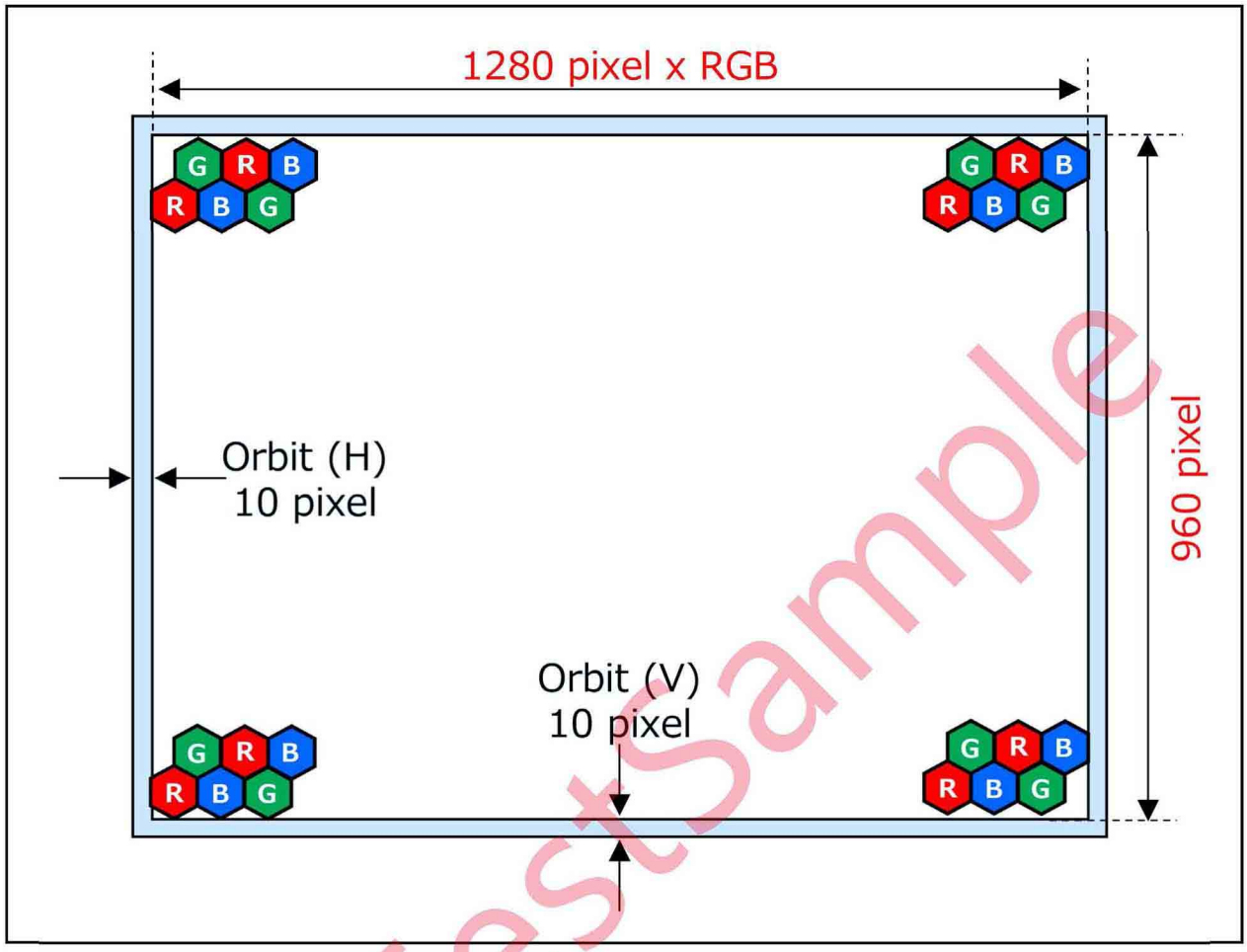


Figure 1-1. Display Structure Diagram

Figure 1-1 shows the structure of this µOLED display.

The video interface of this display conforms to MIPI-DSI v1.2.

2. Device Structure

Table 2-1. Device Structure

Module size		17.88 mm x 15.28 mm x 6.24 mm (not including flexible cable part)
Pixel size		7.8 µm x 7.8 µm
Number of display pixels		1280 (H) x 960 (V)
Number of effective pixels		1300 (H) x 980 (V) (including the orbit area)
Number of orbit area pixels	H	20
	V	20
Effective pixel area size		10.14 mm x 7.64 mm (including the orbit area)

3. Pixel Arrangement

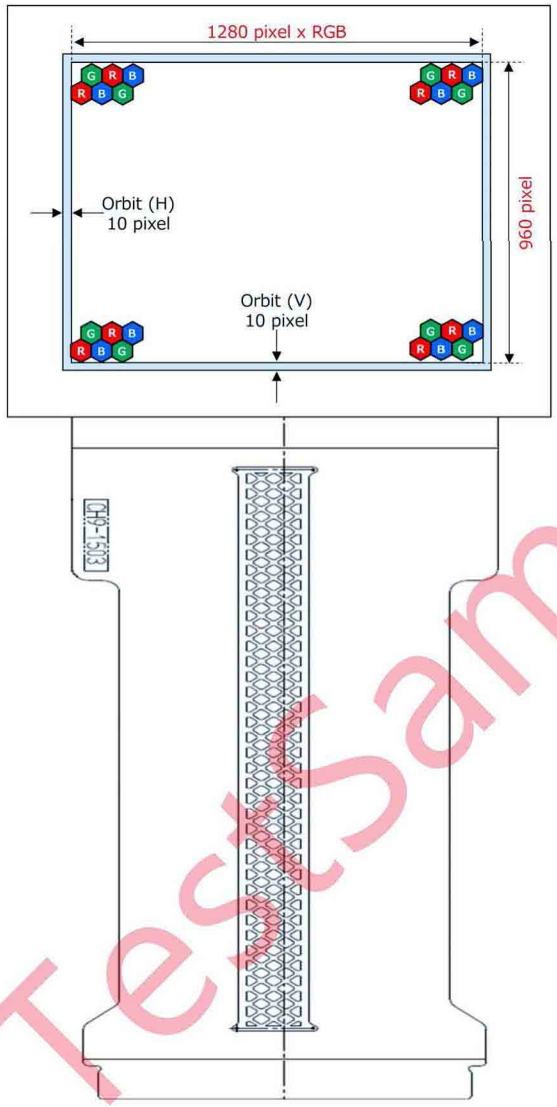


Figure 3-1. Pixel Data Format (Physical Arrangement)

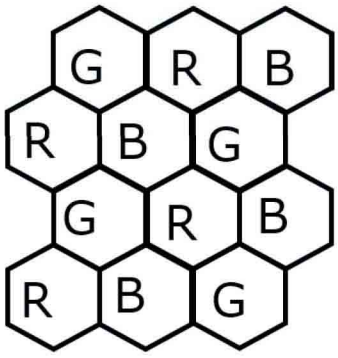


Figure 3-2. Color Filter Arrangement

4. Pin Specifications

Table 4-1. Pin Specifications 1

FPC No.	Pin name	Type	Description	Remarks
01	VDD	P	1.8 V Power Supply	-
02	VSS	G	GND	-
03	VSSE	G	GND	-
04	VSSE	G	GND	-
05	VDDE	P	10 V Power Supply	-
06	VDDE	P	10 V Power Supply	-
07	VDDH	P	10 V Power Supply	-
08	VDD	P	1.8 V Power Supply	-
09	VSS	G	GND	-
10	VSS	G	GND	-
11	Reserved	I	Reserved	Connect with VDD
12	Reserved	I	Reserved	Connect with GND
13	RES_B	I	System reset signal	-
14	CS	I	Chip select	-
15	SCK	I	Serial clock	-
16	SI	I	Serial data input	-
17	SO	O	Serial data output	-
18	Reserved	G	Reserved	Connect with GND
19	Reserved	G	Reserved	Connect with GND
20	Reserved	G	Reserved	Connect with GND
21	Reserved	G	Reserved	Connect with GND
22	Reserved	O	Reserved	No connection
23	Reserved	O	Reserved	No connection
24	VSSIF	G	Interface GND	-
25	VDDIF	P	Interface 1.8 V power supply	-
26	MIPI_D0P	I	MIPI Data0 (Pos)	-
27	MIPI_D0N	I	MIPI Data0 (Neg)	-
28	MIPI_CLKP	I	MIPI CLK (Pos)	-
29	MIPI_CLKN	I	MIPI CLK (Neg)	-
30	MIPI_D1P	I	MIPI Data1 (Pos)	-

<Type>

G: GND pin, P: Power supply pin, I: Input pin, O: Output pin

Table 4-2. Pin Specifications 2

FPC No.	Pin name	Type	Description	Remarks
31	MIPI_D1N	I	MIPI Data1 (Neg)	-
32	MIPI_D2P	I	MIPI Data2 (Pos)	-
33	MIPI_D2N	I	MIPI Data2 (Neg)	-
34	VDDIF	P	Interface 1.8 V power supply	-
35	VSSIF	G	Interface GND	-
36	Reserved	O	Reserved	No connection
37	Reserved	O	Reserved	No connection
38	Reserved	O	Reserved	No connection
39	Reserved	O	Reserved	No connection
40	Reserved	O	Reserved	No connection
41	Reserved	O	Reserved	No connection
42	Reserved	O	Reserved	No connection
43	Reserved	O	Reserved	No connection
44	Reserved	I	Reserved	Connect with GND
45	VSS	G	GND	-
46	VDD	P	1.8 V power supply	-
47	Reserved	O	Reserved	No connection
48	Reserved	O	Reserved	No connection
49	Reserved	O	Reserved	No connection
50	Reserved	I	Reserved	No connection
51	VR1	O	Reference voltage	-
52	VR2	O	Reference voltage	-
53	VR3	O	Reference voltage	-
54	VR4	O	Reference voltage	-
55	VSS	G	GND	-
56	VDD	P	1.8 V power supply	-
57	VDDH	P	10 V power supply	-
58	VDDE	P	10 V power supply	-
59	VDDE	P	10 V power supply	-
60	VSSE	G	GND	-
61	VSSE	G	GND	-

<Type>

G: GND pin, P: Power supply pin, I: Input pin, O: Output pin

15. Package Specifications

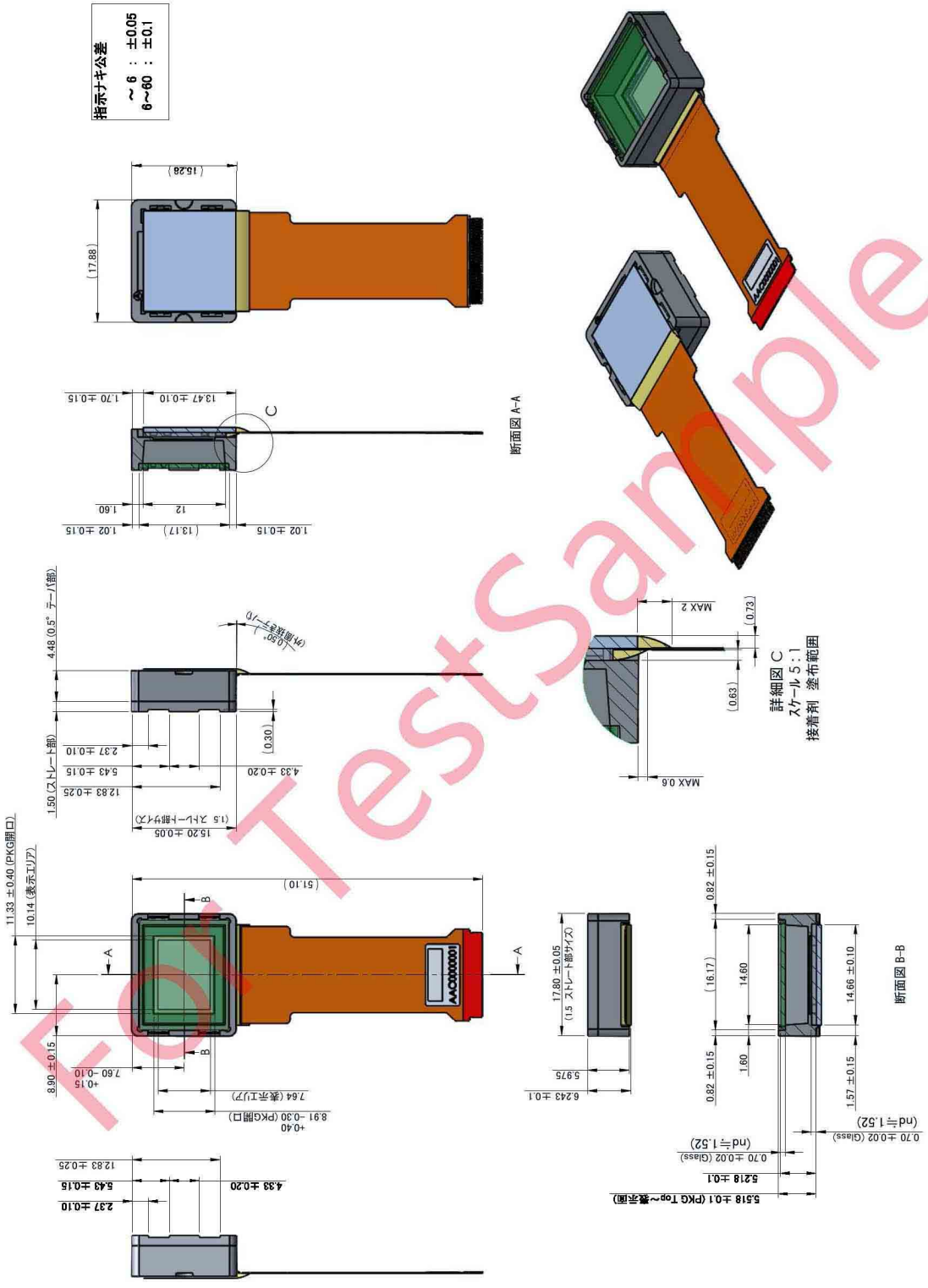


Figure 15-1. Package Specifications (Entire µOLED Module)

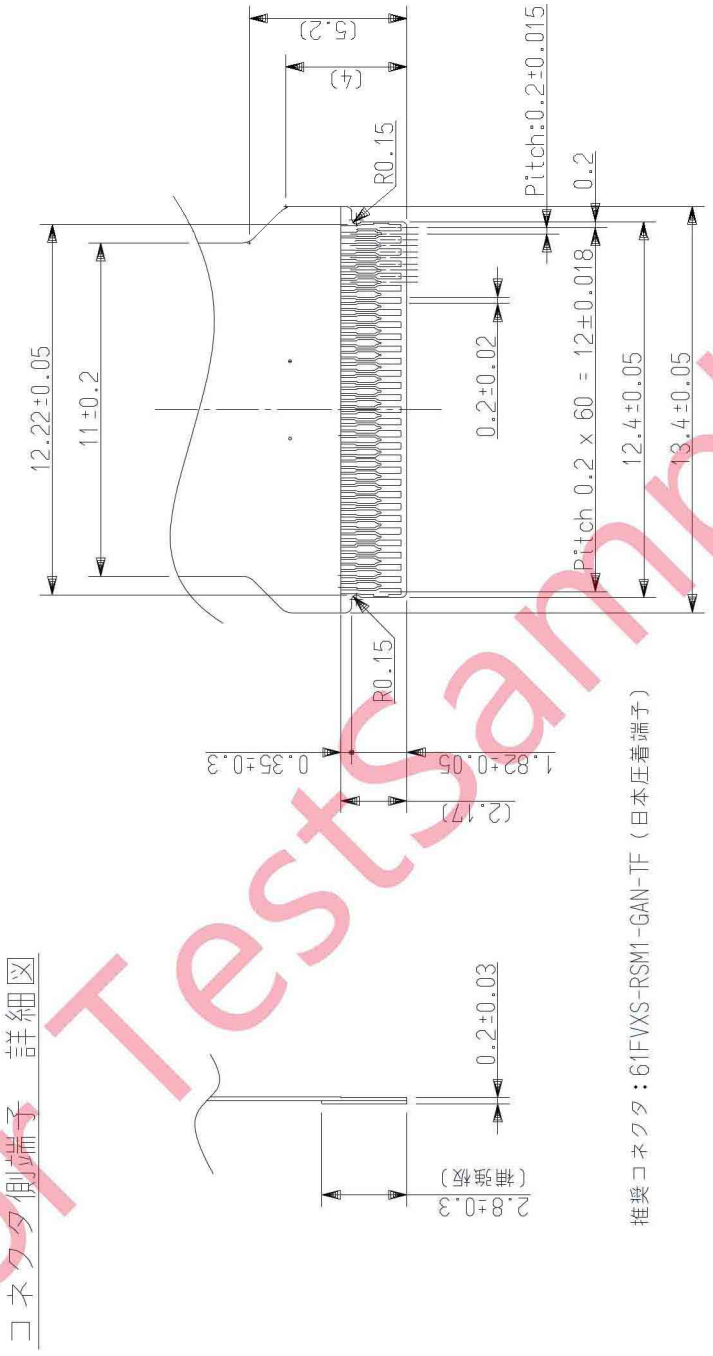


Figure 15-2. imension Diagram (FPC)